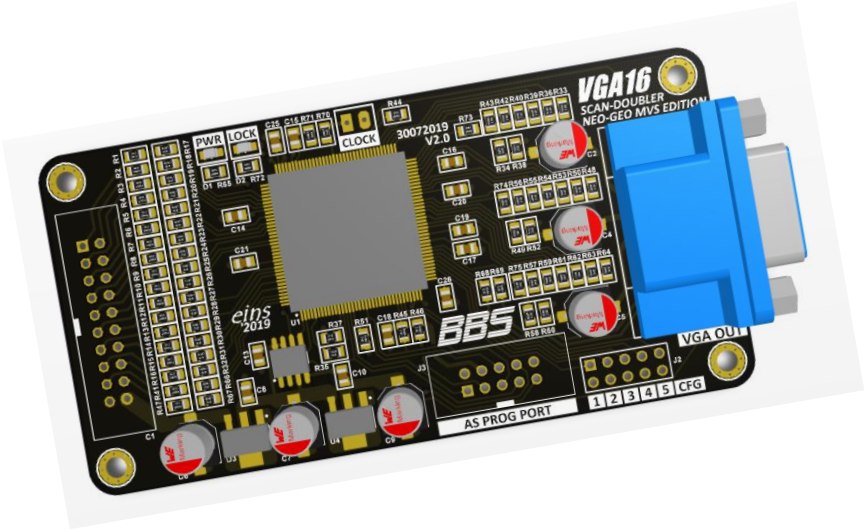
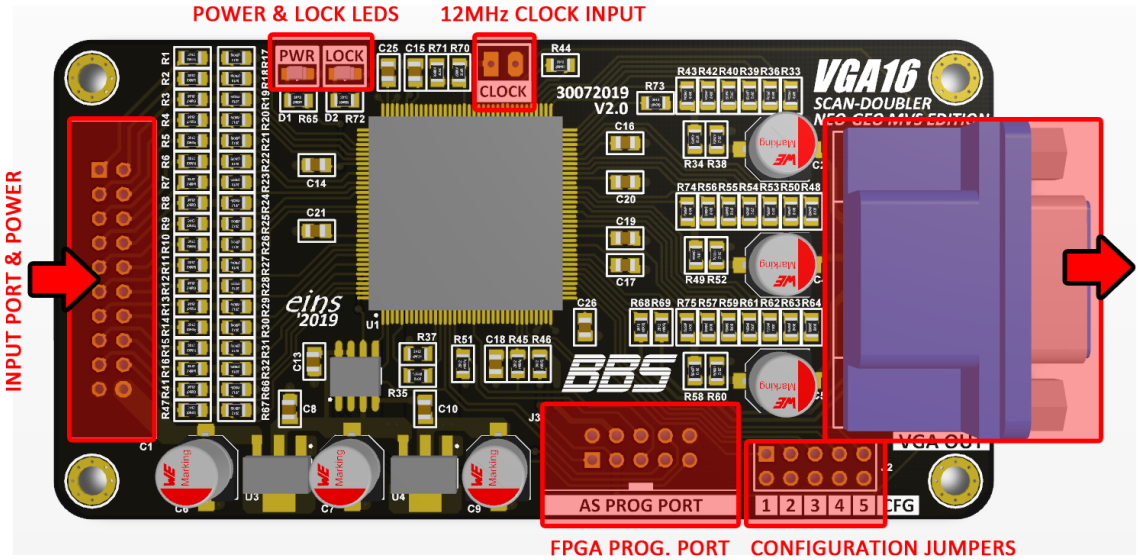


VGA16 samples NEO-GEO's 3x5 Bit Digital RGB, DAK and SHD signals before going to the resistor divider DACs. This data is level shifted and fed to the FPGA for further processing. FPGA captures every scanline and sends to VGA output interface twice. Since NEO-GEO's original video output is NTSC (~30FPS, interlaced, 262.5 lines per field), by using this technic, we are able to generate a 640x480 @60Hz Progressive VGA signal.

Since there are no frame buffers used in this method, there is no noticeable latency. Only one scanline is buffered, and played back twice.

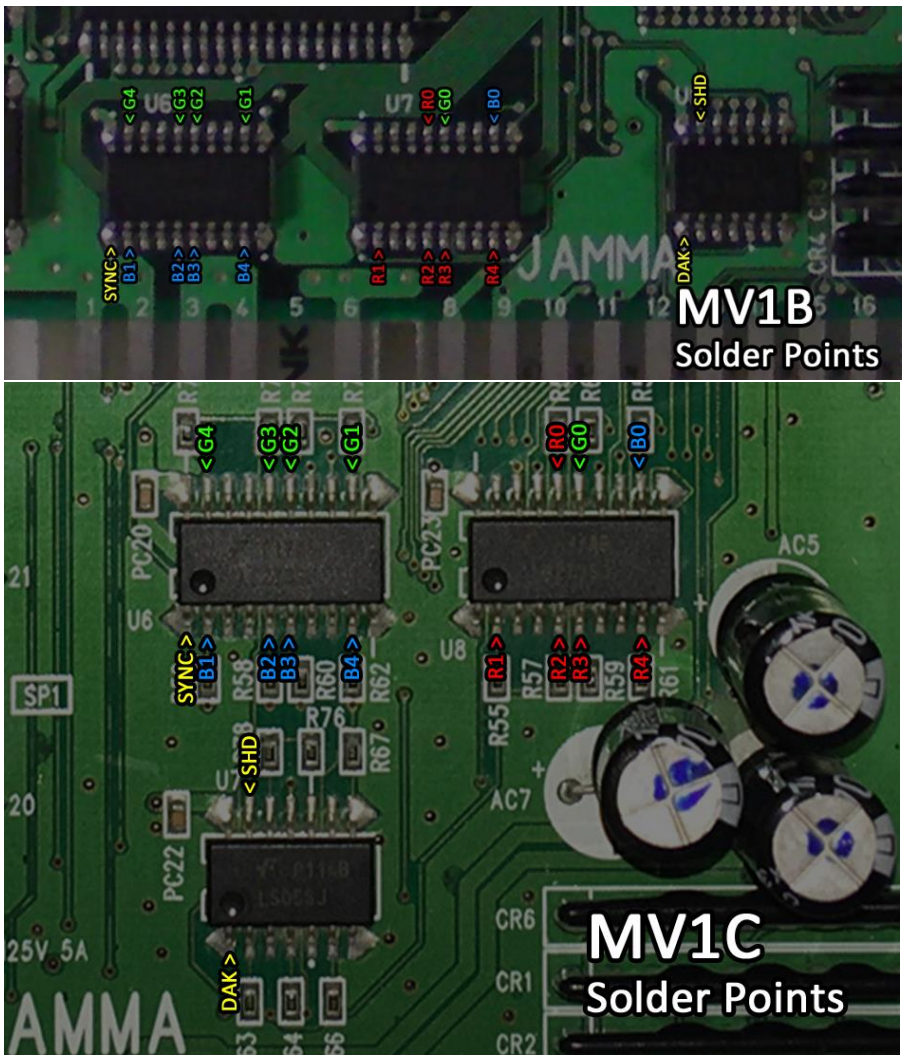
CRT Scanline effects and conversion from RGB to YPbPr is also possible.

VGA16 Layout, Ports and Configuration



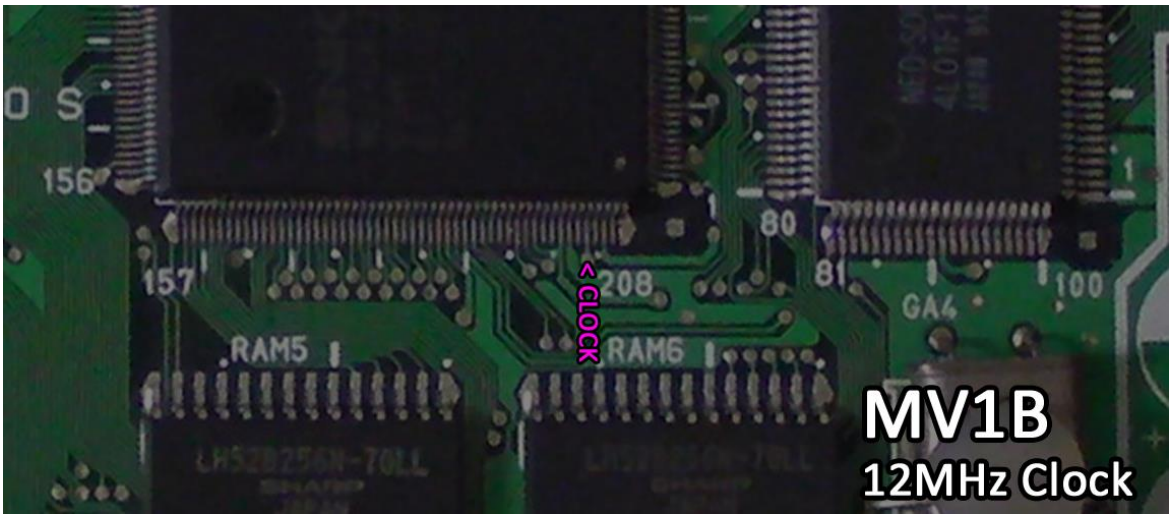
INPUT & POWER PORT				
Pin	**Signal**	**Solder Location (MV1B)**	**Solder Location (MV1C)**	**Hint**
1	R0	U7 Pin 16	U8 Pin 16	Pin routed to 3.9K resistor
2	R1	U7 Pin 2	U8 Pin 2	Pin routed to 2.2K resistor
3	R2	U7 Pin 5	U8 Pin 5	Pin routed to 1K resistor
4	R3	U7 Pin 6	U8 Pin 6	Pin routed to 0.47K resistor
5	R4	U7 Pin 9	U8 Pin 9	Pin routed to 0.22K resistor
6	G0	U7 Pin 15	U8 Pin 15	Pin routed to 3.9K resistor
7	G1	U6 Pin 12	U6 Pin 12	Pin routed to 2.2K resistor
8	G2	U6 Pin 15	U6 Pin 15	Pin routed to 1K resistor
9	G3	U6 Pin 16	U6 Pin 16	Pin routed to 0.47K resistor
10	G4	U6 Pin 19	U6 Pin 19	Pin routed to 0.22K resistor
11	B0	U7 Pin 12	U8 Pin 12	Pin routed to 3.9K resistor
12	B1	U6 Pin 2	U6 Pin 2	Pin routed to 2.2K resistor
13	B2	U6 Pin 5	U6 Pin 5	Pin routed to 1K resistor
14	B3	U6 Pin 6	U6 Pin 6	Pin routed to 0.47K resistor
15	B4	U6 Pin 9	U6 Pin 9	Pin routed to 0.22K resistor
16	DAK	U5 Pin 1	U7 Pin 1	
17	SHD	U5 Pin 13	U7 Pin 13	
18	SYNC	U6 or U7 Pin 1	U6 or U8 Pin 1	
19	GND			
20	+5 VDC			

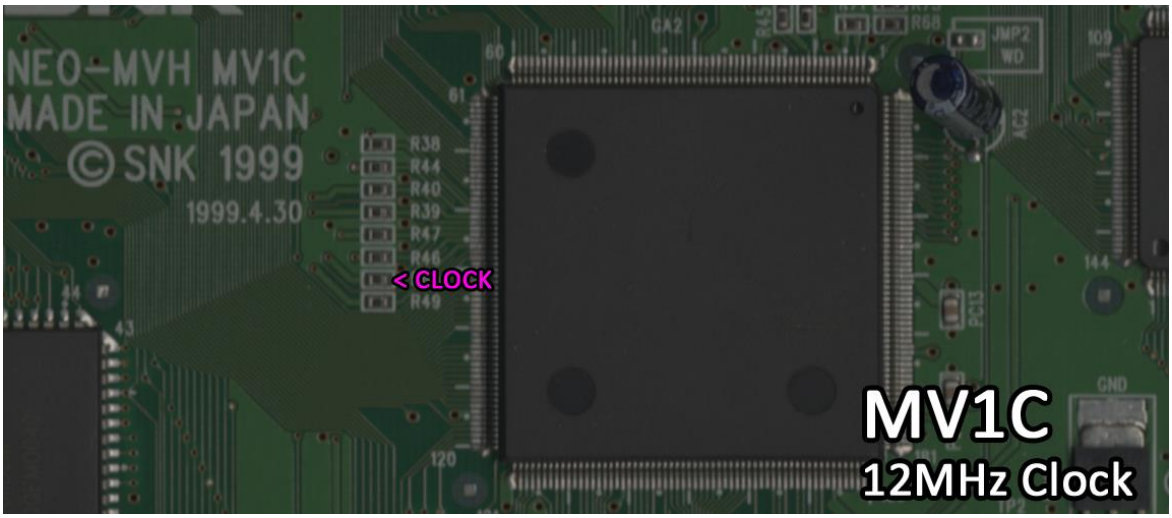
Table 1: RGB Data, DAK, SHD, SYNC & Power Input Pin Definitions



12MHz CLOCK INPUT

A 12MHz synchronous system clock signal is also required. This wire must be as short as possible. BLUE LOCK LED will be lit when proper 12MHz clock is detected and locked into.





POWER & LOCK LEDS

POWER LED will be lit when 5V supply voltage is present. The BLUE LOCK LED will be lit when a proper 12MHz system clock is present and the internal FPGA PLL is locked to this signal. Normally these two LED's should be lit.

FPGA PROG. PORT

This port is used to program the board at factory.

PLEASE DO NOT USE THIS PORT !

CONFIGURATION JUMPERS

JUMPER	Configuration	Description
1-2	**Scanline Effect**	J1:OFF J2:OFF > Scanlines OFF J1:ON J2:OFF > Scanlines Min J1:OFF J2:ON > Scanlines Med J1:ON J2:ON > Scanlines Max
3	**Color Blending Effect**	When this jumper is on position, sucsessive pixel colors are mixed in 1 to 3 ratio to generate analog CRT color blending effect.
4	**Test Pattern**	J4: ON > Test pattern is shown
5	**VGA/YPrPb Output**	J5: ON > Output Signal is VGA J5: OFF > Output Signal is YPbPr

Table 2: Configuration Jumpers

VGA / YPbPr OUTPUT

Output signal format can be configured using configuration jumper *5*.

When the jumper is on, Standard VGA Signal with separate H and V syncs are generated. Output resolution is 640x480 @ 60Hz.

When this jumper is removed, sampled RGB signal is converted to YPbPr signal by the FPGA. Composite sync signal is generated and inserted into Y line.

PIN	YPbPr Mode	VGA Mode
1	Pr	RED Signal
2	Y	GREEN Signal
3	Pb	BLUE Signal
6	GND	GND
7	GND	GND
8	GND	GND
13	N/A	H Sync
14	N/A	V Sync

Table 3: D-SUB15 Output Pin Definitions